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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,833	12/30/2003	Mark A. Anders	P18060	2784

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EXAMINER	
CRAWFORD, JASON	
ART UNIT	**PAPER NUMBER**
2819	

DATE MAILED: 08/21/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/748,833	ANDERS ET AL.	
	Examiner	Art Unit	
	Jason Crawford	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *9 and 10* is/are allowed.

6)☒ Claim(s) *1,2,4,6,11,12,14 and 15* is/are rejected.

7)☒ Claim(s) *3, 5, 7-8 and 13* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. Claim 9 is objected to because of the following informalities: Claim 9 recites the limitation "the full-swing input signal" in line 2 of the claim and "the low-swing signal" in lines 14-15 in the claim. There is insufficient antecedent basis for these limitations in the claims. Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1- 2, 4 and 6 are rejected under 35 U.S.C. 102(b) as being anticipated by Mizukami et al. (US 5,111,080).

In regards to claim 1, Mizukami discloses of a circuit in Fig 1 comprising a static low-swing driver circuit (UBD) to receive a full-swing input signal (IN, swinging from VDD to GND), to convert the full-swing input signal (IN) to a low-swing input signal (a, b, swinging from VDD-Vth to GND), and to transmit the low-swing input signal (a, b) and a dynamic receiver circuit (UBR) to receive the low-swing input signal (a, b) and to convert the low-swing input signal (a, b) to a full-swing signal (OUT, swinging from VDD to GND). (Fig 1 and 2, Column 3 Lines 58-67, Column 4 Lines 1-43 and Column 6 Lines 39-59)

In regards to claim 2, Mizukami discloses of the circuit of claim 1 further comprising an interconnect (TRANSMISSION LINES) coupled to the driver circuit (UBD) and to the receiver circuit (UBR), the interconnect (TRANSMISSION LINES) to receive the low-swing input signal (a, b) from the driver and to transmit the low-swing input signal (a, b) to the receiver circuit (UBR), wherein the interconnect does not comprise a repeater (see Fig 1). (Fig 1 and 2, Column 3 Lines 58-67, Column 4 Lines 1-43 and Column 6 Lines 39-59)

In regards to claim 4, Mizukami discloses of the receiver circuit (UBR) comprising a positive edge-triggered dynamic sense-amplifying (SA circuit in UBR) flip-flop (based on the positive edge of PR, when it is HIGH). (Fig 1, 2, Column 5 Lines 61-67 and Column 6 Lines 1-21)

In regards to claim 6, Mizukami discloses of the receiver circuit (UBR) comprising a true single-phase clock-style positive edge-triggered level-restoring flip-flop (PR is a single phase, clock-style signal and UBR is responsive to PR being HIGH, or on the positive edge). (Fig 1, 2, Column 5 Lines 61-67 and Column 6 Lines 1-21)

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 11-12 and 14-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizukami et al. (US 5,111,080) in view of Zimlich (US 6,972,587).

In regards to claim 11, Mizukami discloses of a circuit in Fig 1 comprising a static low-swing driver circuit (UBD) to receive a full-swing input signal (IN, swinging from VDD to GND), to convert the full-swing input signal (IN) to a low-swing input signal (a, b, swinging from VDD-Vth to GND), and to transmit the low-swing input signal (a, b) and a dynamic receiver circuit (UBR) to receive the low-swing input signal (a, b) and to convert the low-swing input signal (a, b) to a full-swing signal (OUT, swinging from VDD to GND) wherein the circuit is comprised within a processor unit (PU in Fig 7) coupled to a memory unit (MU). (Fig 1, 2 and 7, Column 3 Lines 58-67, Column 4 Lines 1-43, Column 6 Lines 39-59 and Column 10 Lines 51-65)

Mizukami does not directly disclose of the processor memory being double data rate (DDR) memory.

Zimlich discloses of a device (10) including a processor (12) connected to a driver (transmitter) and receiver (in 20, Column 3 Lines 64-66) and coupled to a memory unit (26), that includes DDR memory (Column 4 Lines 9-12). (Fig 1, Column 3 Lines 64-66 and Column 4 Lines 9-12)

At the time the invention was made, it would have been obvious to one of ordinary skill in the art to use DDR memory in a processor as taught by Zimlich to have a non-volatile memory element that retains its value at power down at a speed of double the rate.

In regards to claim 12, Mizukami in view of Zimlich discloses of the system of claim 11 further comprising an interconnect (TRANSMISSION LINES of Mizukami) coupled to the driver circuit (UBD) and to the receiver circuit (UBR), the interconnect (TRANSMISSION LINES) to receive the low-swing input signal (a, b) from the driver and to transmit the low-swing input signal (a, b) to the receiver circuit (UBR), wherein the interconnect does not comprise a repeater (see Fig 1). (Mizukami Fig 1 and 2, Column 3 Lines 58-67, Column 4 Lines 1-43 and Column 6 Lines 39-59)

In regards to claim 14, Mizukami in view of Zimlich discloses of the receiver circuit (UBR of Mizukami) comprising a positive edge-triggered dynamic sense-amplifying (SA circuit in UBR) flip-flop (based on the positive edge of PR, when it is HIGH). (Fig 1, 2, Column 5 Lines 61-67 and Column 6 Lines 1-21 of Mizukami)

In regards to claim 15, Mizukami in view of Zimlich discloses of the receiver circuit (UBR of Mizukami) comprising a true single-phase clock-style positive edge-triggered level-restoring flip-flop (PR is a single phase, clock-style signal and UBR is responsive to PR being HIGH, or on the positive edge). (Fig 1, 2, Column 5 Lines 61-67 and Column 6 Lines 1-21 of Mizukami)

Allowable Subject Matter

4. Claims 9 and 10 are allowed. The following is an examiner's statement of reasons for allowance:

In regards to claim 9, the prior art does not directly disclose of a driver circuit with an inverter and delay element coupled to an input line wherein the output of the inverter

goes to a gate of a first transistor that has *a drain coupled to a first voltage that is lower than the supply voltage* and a second transistor that has a gate coupled to the output of the delay element wherein the *drain of the second transistor is coupled to the source of the first transistor*, nor would it have been obvious to one of ordinary skill to do so. Claim 10 is also allowed as being dependent on the allowable claim 9.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

5. Claims 3, 5, 7-8 and 13 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

In regards to claims 3 and 13, the prior art does not directly disclose of a driver circuit with an inverter and delay element coupled to an input line wherein the output of the inverter goes to a gate of a first transistor that has *a drain coupled to a first voltage that is lower than the supply voltage* and a second transistor that has a gate coupled to the output of the delay element wherein the *drain of the second transistor is coupled to the source of the first transistor*, nor would it have been obvious to one of ordinary skill to do so.

In regards to claim 5, the prior art does not directly disclose of the circuit according to claim 4 comprising a driver input line, *an inverter coupled to a supply voltage, a delay element coupled to the supply voltage wherein the inverter and the delay element are coupled to the input line, a first and second transistor wherein the gate of the first transistor is coupled to an output of the inverter and the gate of the second transistor is coupled to output of the delay element and a driver output line coupled to an output node coupled to the outputs of both transistors*, nor would it have been obvious to one of ordinary skill in the art to do so.

In regards to claim 7, the prior art does not directly disclose the circuit of claim 6 wherein the receiver comprises an input line, *an inverter coupled to V_{SS} and* ***to a first voltage less than V_{SS},*** *the inverter coupled to a clock signal and a pull-up transistor coupled to the output of the inverter and to V_{CC},* nor would it have been obvious to one of ordinary skill in the art to do so. Claim 8 is also objected to as being dependent on claim 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jason Crawford whose telephone number is 571-272-6004. The examiner can normally be reached on Monday - Friday 7am-4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Rex Barnie can be reached on 571-272-7492. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

JMC

JAMES CHO
PRIMARY EXAMINER